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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/945,266	08/31/2001	Richard L. Coulson	42390P11446	3830

8791 7590 01/25/2007
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EXAMINER	
CHOI, WOO H	
ART UNIT	**PAPER NUMBER**
2189	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/25/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/945,266	COULSON, RICHARD L.	
	Examiner	Art Unit	
	Woo H. Choi	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *See Continuation Sheet* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6,9,11-13,15,17-19,21,23,24,26,27,30,32,33,35,42-46,48,51,53 and 57-67* is/are rejected.

7)☐ Claim(s) *4,28 and 34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Continuation of Disposition of Claims: Claims pending in the application are 1-4,6,9,11-13,15,17-19,21,23,24,26-28,30,32-35,42-46,48,51,53 and 57-67.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 – 3, 6, 9, 11, 12, 13, 15, 18, 19, 21, 23, 24, 26, 27, 30, 32, 33, 35, 42 – 45, 48, 51, 53, 57, 59 – 62, and 66, are rejected under 35 U.S.C. 103(a) as being obvious over Ramakrishnan *et al.* (US Patent No. 5,636,355, hereinafter "Ramakrishnan") in view of De Martin *et al.* (US Patent No. 5,619,675, hereinafter "De Martin") and further in view of Davis *et al.* (US Patent Application Publication No. 2003/0023922, hereinafter "Davis").

3. With respect to claims 1, 9, 11, 12, 13, 18, 19, 23, 24, 26, 32, 35, 42 – 45, 48, 51, 53, 57, 59 – 62, and 66, Ramakrishnan discloses a method comprising:

keeping track of least recently used (LRU) information when a memory is accessed to read data (figure 2, 40, 42, 50, reading a dirty block); and

setting a usage bit (dirty block indication) during a writeback cycle to write the read data back to the memory, the usage bit indicating usage information for the read data (23, dirty blocks are purged/writtenback and their dirty indications cleared).

However, Ramakrishnan does not specifically disclose that keeping track of LRU involves checking a current clock period, current clock period being one of a given number of

clock periods. On the other hand, De Martin discloses a method to keep track of LRU information that checks a current clock period (figure 3). De Martin also discloses a different set of usage bits (abstract, claim 2, ICBMs). These bits are set during a writeback cycle in the combined teachings since a writeback operation purges the associated cache entry and consequently the LRU list must be updated.

It would have been obvious to one of ordinary skill in the art, having the teachings of Ramakrishnan and De Martin before him at the time the invention was made, to use De Martin's method of locating LRU cache line in the computer system of Ramakrishnan to reduce memory overhead (De Martin, col. 2, lines 50 – 3).

Ramakrishnan and De Martin disclose all of the limitations of the claims with the exception of a non-volatile destructive magnetic memory. On the other hand, Davis discloses a magnetic random access memory (MRAM), which is a non-volatile destructive magnetic memory, suitable for both short term and long term storage applications (Davis, col. 1, page 1, paragraph 3).

It would have been obvious to one of ordinary skill in the art, having the teachings of Ramakrishnan, De Martin and Davis before him at the time the invention was made, to use the MRAM device in the disk cache design of Ramakrishnan and De Martin, since the MRAM devices have relatively low power consumption and relative fast access time, particularly for data write applications, which renders MRAM devices ideally suitable for both short term and long term storage applications (Davis, paragraph 3).

4. With respect to claims 2, 3, 27 and 33, see De Martin, col. 6, lines 51 – 52.

5. With respect to claims 6, 15, 21, 30, see De Martin, figure 3.

6. Claims 1, 12, 17, 42, 46, 51, 64, 65 are rejected under 35 U.S.C. 103(a) as being obvious over Ramakrishnan and De Martin and further in view of Li *et al.* (US Patent Application Publication No. 2003/0001176, hereinafter "Li").

Ramakrishnan discloses a method comprising:

keeping track of least recently used (LRU) information when a memory is accessed to read data (figure 2, 40, 42, 50, reading a dirty block); and

setting a usage bit (dirty block indication) during a writeback cycle to write the read data back to the memory, the usage bit indicating usage information for the read data (23, dirty blocks are purged/writtenback and their dirty indications cleared).

However, Ramakrishnan does not specifically disclose that keeping track of LRU involves checking a current clock period, current clock period being one of a given number of clock periods. On the other hand, De Martin discloses a method to keep track of LRU information that checks a current clock period (figure 3). De Martin also discloses a different set of usage bits (abstract, claim 2, ICBMs). These bits are set during a writeback cycle in the combined teachings since a writeback operation purges the associated cache entry and consequently the LRU list must be updated.

It would have been obvious to one of ordinary skill in the art, having the teachings of Ramakrishnan and De Martin before him at the time the invention was made, to use De Martin's

method of locating LRU cache line in the computer system of Ramakrishnan to reduce memory overhead (De Martin, col. 2, lines 50 – 3).

Ramakrishnan and De Martin disclose all of the limitations of the claims with the exception of a non-volatile destructive read memory. On the other hand, Li discloses a polymer ferroelectric memory (PFRAM), which is a non-volatile destructive read memory (Li, abstract).

It would have been obvious to one of ordinary skill in the art, having the teachings of Ramakrishnan, De Martin and Li before him at the time the invention was made, to use the PFRAM device in the disk cache design of Ramakrishnan and De Martin, because of its low power and non-volatile characteristics (Li, paragraph 6). Li also discloses that, unlike flash memory, PFRAM may obviate the need for charge pump or other high-voltage memory technologies (paragraph 56).

7. Claims 1, 12, 42, 51, 58, 63 and 67 are rejected under 35 U.S.C. 103(a) as being obvious over Ramakrishnan and De Martin and further in view of Morisaki *et al.* (US Patent No. 6,236,586, hereinafter "Morisaki").

Ramakrishnan and De Martin disclose all of the limitations of the claims with the exception of a non-volatile destructive read memory as discussed above. On the other hand, Morisaki discloses a core memory (Morisaki, title and abstract), which is a non-volatile destructive read memory.

It would have been obvious to one of ordinary skill in the art, having the teachings of Ramakrishnan, De Martin and Morisaki before him at the time the invention was made, to use

the core device in the disk cache design of Ramakrishnan and De Martin, because it provides high-speed large-capacity non-volatile storage at low cost (abstract).

Allowable Subject Matter

8. Claims 4, 28, and 34 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Woo H. Choi whose telephone number is (571) 272-4179. The examiner can normally be reached on M-F, 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Woo H. Choi
January 17, 2007